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EXAMINER	
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ART UNIT	PAPER NUMBER
2615	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,267	LIU, TINA Y.	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Afghahi (US Patent # 6,747,695).

[Claim 8]

Afghahi teaches an integrated imager (col. 2 lines 20-21, figure 1) comprising an array of active pixel sensors arranged in rows and columns (figure 1, element 105), a differential amplifier (col. 8 lines 34-37), a multiplexed readout method comprising storing a first APS pixel signal value from a first column of said array of active pixel sensors to form a stored first APS pixel signal value, storing a second APS pixel signal value from a second column of said array of active pixel sensors to form a stored second APS pixel signal value; coupling said stored first APS pixel signal value to said differential gain amplifier and coupling said stored second APS pixel signal value to said differential gain amplifier (col. 5 lines 57-67, col. 6 lines 1-4, figure 5 discloses a multiplexed column for four pixel columns).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of McDaniel (US Patent # 4,996,413).

[Claim 1]

Applicant's admitted prior art teaches a semiconductor-imaging chip (figure 2a, element 200) comprising an array of active pixel sensors (figure 2a, element 218) arranged in rows (figure 2a, element 220) and columns (figure 2a, element 222), an output terminal (figure 3). Applicant's admitted prior art fails to teach a multiplexed column buffer having a plurality of input terminals coupled to a respective plurality of said columns and a multiplexed column buffer output terminal coupled to said output terminal. However Mcdaniel et al. teaches a multiplexed column buffer (figure 4, elements 56, 58, 60, MUXA) having a plurality of input terminals (figure 4, elements 1,5,9) coupled to a respective plurality of columns and a multiplexed column buffer output terminal coupled to said output terminal (col. 3 lines 53-68, col. 6 lines 1-25). Therefore taking the combined teachings of Applicant's admitted prior art and Mcdaniel it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a multiplexed column buffer having a plurality of input terminals coupled to a respective plurality of said columns and a multiplexed column buffer output terminal coupled to said output terminal in order to combine the outputs from the respective columns. The benefit of doing so would be to have a faster readout when some of the columns are combined as taught in Mcdaniel (col. 4 lines 49-54).

[Claim 2]

Applicant's admitted prior art teaches a summing amplifier (figure 5, element 78), which receives the output of the four multiplexers and thus is read as a differential gain amplifier.

[Claims 3 and 11]

McDaniel discloses multiplexed buffer 82 storing digital output and outputting it to an output bus (figure 5) but is silent as to whether this buffer can be used as an amplifier to drive the output bus. However, Official notice is taken of the fact that the buffer can be used as an amplifier in order to save the area on the chip. Therefore taking the combined teachings of Applicant's admitted prior art, Mcdaniel and Official notice, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used the buffer as an amplifier to drive the output bus in order to save some area on the chip.

[Claim 10]

Applicant's admitted prior art teaches a semiconductor-imaging chip (figure 2a, element 200) comprising an array of active pixel sensors (figure 2a, element 218) arranged in rows (figure 2a, element 220) and columns (figure 2a, element 222), an output terminal (figure 3).

Applicant's admitted prior art fails to teach a multiplexed column buffer having a plurality of input terminals and a respective output terminal, said multiplexed column buffer further including a differential gain amplifier selectively connected to at least two of said plurality of input terminals so as to be multiplexed among at least two of said columns wherein said plurality of input terminals of said multiplexed column buffer is

respectively coupled to said plurality of said columns and said multiplexed column buffer output terminal is coupled to said output terminal.

However Mcdaniel et al. teaches a multiplexed column buffer (figure 4, elements 56, 58, 60, MUXA) having a plurality of input terminals (figure 4, elements 1,5,9) and a respective output terminal (figures 4 and 5), said multiplexed column buffer further including a differential gain amplifier (figure 5, element 78, which receives the output of the four multiplexers and thus is read as a differential gain amplifier) selectively connected to at least two of said plurality of input terminals so as to be multiplexed among at least two of said columns (figures 4 and 5) wherein said plurality of input terminals (figure 4, elements 1,5,9) of said multiplexed column buffer (figure 4, elements 56, 58, 60, MUXA) is respectively coupled to said plurality of said columns (figure 3) and a multiplexed column buffer output terminal coupled to said output terminal (col. 3 lines 53-68, col. 6 lines 1-25).

Therefore taking the combined teachings of Applicant's admitted prior art and Mcdaniel it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a multiplexed column buffer having a plurality of input terminals and a respective output terminal, said multiplexed column buffer further including a differential gain amplifier selectively connected to at least two of said plurality of input terminals so as to be multiplexed among at least two of said columns wherein said plurality of input terminals of said multiplexed column buffer is respectively coupled to said plurality of said columns and said multiplexed column buffer output terminal is coupled to said output terminal The benefit of doing so would be to have a

faster readout when some of the columns are combined as taught in Mcdaniel (col. 4 lines 49-54).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, McDaniel (US Patent # 4,996,413) and in further view of Nair et al. (US Patent # 6,366,320).

[Claim 4]

Applicant's admitted prior art teaches a semiconductor-imaging chip (figure 2a, element 200) comprising an array of active pixel sensors (figure 2a, element 218) arranged in rows (figure 2a, element 220) and columns (figure 2a, element 222).

Applicant's admitted prior art fails to teach a multiplexed column buffer comprising first and second memory elements, respective first, second, third and fourth switches, a differential gain amplifier, said first and second switches coupling said first and second memory element to a first and second column of active pixel sensors, said third and fourth switches coupling said differential gain amplifier to said first and second memory elements.

However McDaniel et al teaches a multiplexed column buffer (figures 4 and 5) comprising first and second first and second memory elements (figure 4, element 60), respective first, second, third and fourth switches (figure 3, element 41'), a differential gain amplifier (figure 5, element 78), said first and second switches coupling said first and second memory element to a first and second column of active pixel sensors (figures 3 and 4).

Therefore taking the combined teachings of Applicant's admitted prior art and Mcdaniel it would have been obvious to one skilled in the art at the time of the invention

to have been motivated to have a multiplexed column buffer having a first and second memory elements, respective first, second, third and fourth switches, a differential gain amplifier, said first and second switches coupling said first and second memory element to a first and second column of active pixel sensors. The benefit of doing so would be to have a faster readout when some of the columns are combined as taught in Mcdaniel (col. 4 lines 49-54).

Applicant's admitted prior art in view of Mcdaniel fail to teach third and fourth switches coupling said differential gain amplifier to said first and second memory elements. However Nair et al. teaches third and fourth switches (figure 5, element 520) coupling the differential gain amplifier (the output of switches 520 is shown as input as differential signal pair) to first and second memory elements (C_{SA1} and C_{SA2}).

Therefore taking the combined teachings of Applicant's admitted prior art and Mcdaniel it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have third and fourth switches coupling said differential gain amplifier to said first and second memory elements in order to control the output of the sensor array via switches. The benefit of doing so would be to have the data buffered in the capacitors and being output to the differential amplifier via an output control by operating switches.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, McDaniel (US Patent # 4,996,413) and in further view of Zhou et al. (US Patent # 5,965,871).

[Claims 5 and 6]

Applicant's admitted prior art teaches a semiconductor-imaging chip (figure 2a, element 200) comprising an array of active pixel sensors (figure 2a, element 218) arranged in rows (figure 2a, element 220) and columns (figure 2a, element 222).

Applicant's admitted prior art fails to teach a multiplexed column buffer comprising first and second memory elements, respective first and second switches a bus driver amplifier having respective input and output terminals; said first memory element being coupled to a first column of said array of active pixel sensors; said second memory element being coupled to a second column of said array of active pixel sensors; said first switch coupling said first memory element to said input terminal of said bus driver amplifier; said second switch coupling said second memory element to said input terminal of said bus driver amplifier; and said output terminal of said bus driver amplifier being coupled to said output bus terminal of said semiconductor imaging chip.

However McDaniel et al teaches a multiplexed column buffer (figures 4 and 5) comprising first and second first and second memory elements (figure 4, element 60), respective first and second switches (figure 3, element 41'), said first and second memory elements coupling to a first and second column of active pixel sensors (figures 3 and 4). McDaniel discloses buffer 82 storing digital output and outputting it to an output bus (figure 5) but is silent as to whether this buffer can be used as an amplifier to drive the output bus. However, Official notice is taken of the fact that the buffer can be used as an amplifier in order to save the area on the chip.

Applicant's admitted prior art in view of McDaniel fail to teach first and second switches being used to couple the bus driver amplifier with the first and second memory elements through the differential amplifier. However Zhou et al. disclose first and second

switches (figure 3, elements 56 and 76) used to couple the output circuit 25 with the first and second memory elements (figure 3, elements 54 and 74). Therefore taking the combined teachings of Applicant's admitted prior art, Mcdaniel and Zhou et al., it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have first and second switches being used to couple the bus driver amplifier with the first and second memory elements through the differential amplifier. The benefit of doing so would be to have a multiplexed column buffer architecture, which can be used for a fast readout.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US Patent # 5,965,871).

[Claim 9]

Zhou et al. teaches an integrated imager (figure 1) comprising an array of active pixel sensors arranged in rows and columns (figure 1, element 14), said integrated imager including a pattern cancellation circuit (figure 3) for providing a corrected APS pixel signal value (col. 9 lines 30-44). Zhou et al. is silent as to the semiconductor-imaging chip further including at least one bus driver amplifier, and output bus terminal. However Official notice is taken of the fact that a bus driver amplifier, and output bus terminal is notoriously common in an imager chip in order to amplify the data and output the data from the chip. Zhou et al. teaches a multiplexed readout method (col. 4 lines 23-24, figures 1 and 3, element 20 and 22) comprising storing a first corrected APS pixel signal value, storing a second corrected APS pixel signal value, coupling said stored first corrected APS pixel signal value to said bus driver amplifier (col. 5 lines 62-67, col. 6 lines 1-7) and coupling said stored second corrected APS signal value to said bus driver

amplifier (col. 9 lines 30-44, figures 3 and 4 show for one column but it is the same FPN cancellation circuit for all the columns).

Allowable Subject Matter

8. Claim 7 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fail to suggest fairly respective first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth memory elements; respective first, second, third, fourth, fifth and sixth switches, a differential gain amplifier having respective first and second input terminals and a respective output terminal, a bus driver amplifier having respective input and output terminals; said first switch coupling said first memory element to a first column of said array of active pixel sensors; said second switch coupling said second memory element to the said first column of said array of active pixel sensors; said third switch coupling said third memory element to said second column of said array of active pixel sensors, said fourth switch coupling said fourth memory element to said second column of said array of active pixel sensors; said fifth switch coupling said first memory element to said first input terminal of said differential gain amplifier, said sixth switch coupling said third memory element to said first input terminal of said differential gain amplifier; said seventh switch coupling said second memory element to said second input terminal of said differential gain amplifier; said eighth switch coupling said fourth memory element to said second input terminal of said differential gain amplifier; said ninth switch coupling said fifth memory element to said output terminal of said differential gain amplifier; said tenth switch coupling said sixth memory element to said output terminal of said differential gain amplifier; said eleventh

switch coupling said fifth memory element to said input terminal of said bus driver amplifier; said twelfth switch coupling said sixth memory element to said input terminal of said bus driver amplifier; and said output terminal of said bus driver amplifier being coupled to said output terminal of said semiconductor imaging chip.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
September 10, 2004

TUAN HO
PRIMARY EXAMINER